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DECOD$5	0
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DECODAGEZI	1
DECODAGEZ1	1
DECODAGEZ2	1
DECODAGEZ3	1
(L52 AND DECOD$5).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	1

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L53	L52 and decod$5	1	L53
L52	L51 and (map$5 or interrupt$5)	1	L52
L51	l33 and sram	1	L51
L50	l48 and look$7	1	L50
L49	L48 and permut$7	0	L49
L48	L47 and floating	1	L48
L47	L46 and (counter$1 or branch$3 or cache)	1	L47
L46	L45 and vliw	1	L46
L45	L33 and dispatch$5	1	L45
L44	L43 and stor$3	1	L44
L43	L42 and load$3	1	L43
L42	l33 and (external$3 or main)	1	L42
L41	l33 and external$3 or main	3019739	L41
L40	dram$1 and l37	1	L40
L39	L37 and 35	1	L39
L38	L37 and 36	0	L38
L37	5822606.pn.	2	L37
L36	external$3 near4 dram$1 near8 host near25 (chip or chipset or IC)	32	L36
L35	external$3 near4 dram$1 near8 host	69	L35

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L34	L33 and pci and I near1 O	1	L34
L33	5909559.pn.	1	L33
L32	l12 and l27	4	L32
L31	l12 and l26	4	L31
L30	l3 and l28	0	L30
L29	l3 and l26	1	L29
L28	(709/238-244)[CCLS]	4174	L28
L27	(710/305-317)[CCLS]	4995	L27
L26	(710/305-317)![CCLS]	4995	L26

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L25	L21 and l10	.0	L25
L24	L21 and l9	1	L24
L23	L21 and l7	0	L23
L22	L21 and l6	4	L22
L21	l1 and (north or south)	83	L21
L20	l3 and l10	1	L20
L19	l3 and l9	5	L19
L18	l3 and l7	18	L18
L17	l3 and l6	35	L17
L16	L12 and l10	0	L16

L15	L12 and l9	5	L15
L14	L12 and l7	10	L14
L13	L12 and l6	41	L13
L12	(chip or chipset or IC) and (vector) and scalar and host$3 and (north or south)	282	L12
L11	(chip or chipset or IC) and (vector) and scalar and host$3 and (north or south) near4 bridg$4	26	L11

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L10	(712/38)[CCLS]	179	L10
L9	(712/28-40)[CCLS]	1962	L9
L8	(712/2-9)[CCLS]	458	L8
L7	(712/2-9)[CCLS]	458	L7
L6	(712/2-300)[CCLS]	12434	L6

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L5	L3 and host$3	18	L5
L4	L3 and host$3 near18 external$3	14	L4
L3	(chip or chipset or IC) near25 (vector) near20 scalar	63	L3
L2	L1 and (vector) and scalar	19	L2
L1	(chip or chipset or IC) near15 host$3 near18 external$3	802	L1

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                                                        30 April-2 May 1996 Page(s):261 - 268
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